

L Number	Hits	Search Text	DB	Time stamp
-	756	(system cpu) near10 (read near5 (latency delay))	USPAT; US-PGPUB; EPO; JPO	2004/07/15 15:47
-	965	device near10 (read near7 (latency delay))	USPAT; US-PGPUB; EPO; JPO	2004/07/15 15:31
-	67	((system cpu) near10 (read near5 (latency delay))) same (device near10 (read near7 (latency delay)))	USPAT; US-PGPUB; EPO; JPO	2004/07/15 15:23
-	8	sum near10 (device near4 read near4 latency)	USPAT; US-PGPUB; EPO; JPO	2004/07/26 09:54
-	8	sum near10 (device near4 read near4 latenc\$3)	USPAT; US-PGPUB; EPO; JPO	2004/07/15 15:29
-	7	((system cpu) near10 (read near5 (latency delay))) and (sum near10 (device near4 read near4 latenc\$3))	USPAT; US-PGPUB; EPO; JPO	2004/07/15 15:29
-	7	((system cpu) near10 (read near5 (latency delay))) same (sum near10 (device near4 read near4 latenc\$3))	USPAT; US-PGPUB; EPO; JPO	2004/07/15 15:29
-	11	(sum\$3 add\$3) near10 (device near4 read near4 latency)	USPAT; US-PGPUB; EPO; JPO	2004/07/15 15:31
-	24	(device near10 (read near7 (latency delay))) near10 maximum	USPAT; US-PGPUB; EPO; JPO	2004/07/15 15:32
-	55	(minimum near5 read near3 (latency delay)) and (memory near5 (module banks))	USPAT; US-PGPUB; EPO; JPO	2004/07/15 15:47
-	1570	((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))	USPAT; US-PGPUB; EPO; JPO	2004/07/15 15:48
-	114	711/167 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks)))	USPAT; US-PGPUB; EPO; JPO	2004/08/24 11:05
-	1013	711/169	USPAT; US-PGPUB; EPO; JPO	2004/07/23 11:56
-	2376	365/194	USPAT; US-PGPUB; EPO; JPO	2004/07/23 11:56
-	1405	(minimiz\$3 reduc\$3) near10 (delay near5 (access read write))	USPAT; US-PGPUB; EPO; JPO	2004/07/23 11:58
-	3927	(minimiz\$3 reduc\$3) same (delay near10 (access read write))	USPAT; US-PGPUB; EPO; JPO	2004/07/23 11:58
-	65	(system near5 clock) same (((minimiz\$3 reduc\$3) same (delay near10 (access read write))))	USPAT; US-PGPUB; EPO; JPO	2004/07/23 12:08
-	44	(equaliz\$3 compesat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 ((read write access) near6 latency)	USPAT; US-PGPUB; EPO; JPO	2004/07/26 09:54
-	96	(equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 ((read write access) near6 latency)	USPAT; US-PGPUB; EPO; JPO	2004/07/23 12:10
-	172	minimum near8 (device memory) near9 latency	USPAT; US-PGPUB; EPO; JPO	2004/07/23 12:11
-	12	((equaliz\$3 compensat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 ((read write access) near6 latency)) and (minimum near8 (device memory) near9 latency)	USPAT; US-PGPUB; EPO; JPO	2004/07/23 12:11

-	1	6658523.pn.	USPAT; US-PGPUB; EPO; JPO	2004/07/26 09:53
-	2376	365/194	USPAT; US-PGPUB; EPO; JPO	2004/07/26 09:54
-	44	((equaliz\$3 compesat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 ((read write access) near6 latency)	USPAT; US-PGPUB; EPO; JPO	2004/07/26 10:33
-	10	((equaliz\$3 compesat\$3 stabiliz\$3 offset\$4 counterbalanc\$3) near10 ((read write access) near6 latency)) and 365/194	USPAT; US-PGPUB; EPO; JPO	2004/07/26 09:55
-	11	(equaliz\$3 leveliz\$3) near10 ((read write access) near6 latency)	USPAT; US-PGPUB; EPO; JPO	2004/07/26 10:35
-	30	(equaliz\$3 leveliz\$3) same ((read write access) near6 latencies)	USPAT; US-PGPUB; EPO; JPO	2004/07/26 10:35
-	8	(memory near10 devices) same ((equaliz\$3 leveliz\$3) same ((read write access) near6 latencies))	USPAT; US-PGPUB; EPO; JPO	2004/07/26 11:26
-	0	"20030023815"	USPAT	2004/07/26 11:32
-	1	"20030023815"	US-PGPUB	2004/07/26 11:32
-	0	711/105 same "2"	USPAT; US-PGPUB; EPO; JPO	2004/08/24 11:04
-	63	minimum near4 read near10 latency	USPAT; US-PGPUB; EPO; JPO	2004/08/24 11:03
-	9	711/105 and (minimum near4 read near10 latency)	USPAT; US-PGPUB; EPO; JPO	2004/08/24 11:04
-	10	711/167 and (minimum near4 read near10 latency)	USPAT; US-PGPUB; EPO; JPO	2004/08/24 11:04
-	5	711/169 and (minimum near4 read near10 latency)	USPAT; US-PGPUB; EPO; JPO	2004/08/24 11:04
-	4	711/170 and (minimum near4 read near10 latency)	USPAT; US-PGPUB; EPO; JPO	2004/08/24 11:04
-	10	365/194 and (minimum near4 read near10 latency)	USPAT; US-PGPUB; EPO; JPO	2004/08/24 11:04
-	91	365/194 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks)))	USPAT; US-PGPUB; EPO; JPO	2004/08/24 11:05
-	53	711/169 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks)))	USPAT; US-PGPUB; EPO; JPO	2004/08/24 11:05
-	91	365/194 and (365/194 and (((minimum maximum) near5 (latency delay)) and (memory near5 (module banks))))	USPAT; US-PGPUB; EPO; JPO	2004/08/24 11:05